SIMULATION AND TEST RESULTS OF 4-CHANNEL LOW NOISE RAIL-TO-RAIL OPERATIONAL AMPLIFIER ARD824 BASED ON AD824 PROTOTYPE

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Abstract. A 4-channel low noise rail-to-tail operation amplifier chip aRD824 was developed based on Analog Devices AD824 prototype. The operation amplifier is planned to hold low voltage noise < 4 μV for 0.1 Hz to 10 Hz input, low input bias current < 15 pA, and offset voltage < 0.5 mV. The aRD824 contained modified electric scheme modules of AD824. The modification was initiated by the limitation of the producer "Integral" to obtain proper quality FETs. The electric scheme of aRD824 was simulated in PSpice software, and data were compared to the datasheet of AD824. Simulated signals included – open-loop gain dependence on the signal frequency with no load, small signal response with no load, open-loop gain and small signal response for capacitor load 200 pF, slow rate for 10 kΩ resistance load, input bias current vs. temperature, common-mode rejection vs. frequency, and power supply rejection vs. frequency. A square topology of aRD824 was developed that is more compact than the rectangular topology of AD824. Chips of aRD824 were produced and tested on several performance indicators - power supply rejection ratio vs. frequency, small signal response for load 100 pF and 10 kΩ, open loop gain vs. frequency for load 15 pF and 100 kΩ, and output voltage to supply rail vs. sink and source load currents. The measured voltage noise for 0.1 Hz to 10 Hz signal input was 1μV. The experimental results were compared to the datasheet of AD824. A preliminary conclusion was made that aRD824 achieves most of its planned performance parameters and can be accepted as a good analog to AD824. For the final conclusion, additional parameters of aRD824 should be measured to cover all characteristics given in the datasheet of AD824.

Keywords: operational amplifier, AD824, electric scheme, rail-to-rail.

Introduction

In the 90-ties the company Analog Devices developed technology for vertical pnp and npn transistors, which was called complementary bipolar (CB) [1]. This technology allowed to improve significantly various chip solutions, including operational amplifiers. Based on this technology, the company Analog Devices developed various operational amplifiers – AD820 (1993), AD822 (1994), AD823 (1995), AD824 (1995) [2]. They demonstrated extraordinary characteristics for operational amplifiers with respect to the input current, noise level, good dynamics, and low current consumption. These amplifiers did not have the highest available characteristics for their individual parameters, but together they appeared to be very useful for many applications, like photonics [3; 4] and medicine [5; 6], especially where low-level input current is required.

The task for developers of this research was to construct and test a 4-channel low noise rail-to-rail operation amplifier aRD824 with the specification given in Table 1, based on an initial prototype Analog Devices AD824 chip. AD824 is a low-power single polarity Rail to Rail in exit [7] 4-channel operational amplifier [8; 9] with n-channel FET transistors at the input. The production of chips for aRD824 was planned to be realized at the production facility "Integral" in Belarus. Due to limitations and specificity of production processes in this facility, the construction of a chip that uses an electric scheme of AD824 prototype is not applicable as a high rate of damaged chips may occur. Therefore, a modified electric scheme of AD824 prototype was proposed that allows to reach the expected specification.

Table 1

Planned specification of the developed operational amplifier aRD824 chip and actual specification of Analog Devices AD824 chip

Parameter	aRD824 (planned)		AD824 [9]			Units
	Minimal values	Maximal values	Minimal values	Typical	Maximal values	
Offset Voltage T_{MIN} to T_{MAX}	-0.5 -0.8	0.5 0.8	-	0.1	1.0	mV
Input Bias Current T_{MIN} to T_{MAX}	-	15 4000	-	2 300	12 4000	pA

Table 1 (continued)

Parameter	aRD824 (planned)		AD824 [9]			Units
	Minimal values	Maximal values	Minimal values	Typical	Maximal values	
Input Offset Current T_{MIN} to T_{MAX}	- -	10 300	- -	2 300	10 -	pA
Large Signal Voltage Gain R_L = 2 kΩ R_L = 10 kΩ R_L = 100 kΩ T_{MIN} to T_{MAX}, R_L = 100 kΩ	 20 50 250 180	-	 20 50 250 180	 40 100 1000 400	-	$V \cdot mV^{-1}$
Output Voltage (High) I_{SOURCE} = 20 μA I_{SOURCE} = 2.5 mA	 4.975 4.800	-	 4.975 4.800	 4.988 4.985	-	V
Output Voltage (Low) I_{SOURCE} = 20 μA I_{SOURCE} = 2.5 mA	 - -	 25 150	- 	 15 120	 25 150	mV
Voltage noise 0.1 Hz to 10 Hz	-	4	-	2	-	μV p-p

Materials and methods

The electric scheme of AD824 chip was derived from its datasheet [2] and from visual observations of its physical structure. Then several sample modules of the electric scheme were produced at the technological line of "Integral". It appeared that the useful output of such modules is low, mainly due to damages in FETs. Therefore, an updated electric scheme for operation amplifier aRD824 was proposed that reduced the need for FETs. The input stage module got additional source repeaters. The second stage module was modified to be more symmetric. The output stage module obtained additional resistors and capacitors to achieve a frequency compensation. Fig. 1 and Fig. 2 show an example of the modification of modules of the electric scheme – simplified schemes for a current reference module of AD824 and aRD824.

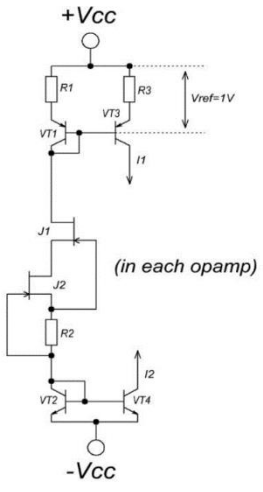

Fig. 1. **Electric scheme of a current reference module of AD824:** *Vcc* – supply voltage; *Vref* – reference voltage; VT1-VT4 – transistors; J1, J2 – FET transistors; R1 – R3 – resistors; I1, I2 – currents

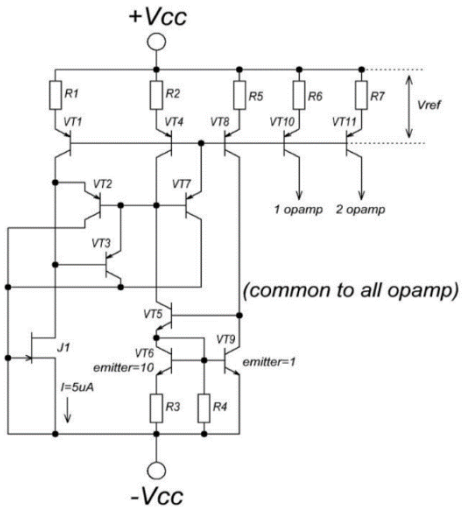

Fig. 2. **Electric scheme of a current reference module of aRD824:** *Vcc* – supply voltage; *Vref* – reference voltage; VT1-VT11 – transistors; J1 – FET transistor; R1-R7 – resistors; *I* – current

Fig.1 shows two FET transistors – J1 and J2. In Fig. 2 only one FET transistor J1 is left, which has low requirements for its quality. PSpice software [10, 11] was used to simulate the electric scheme of aRD824. The obtained results were compared to the datasheet of AD824 [2].

The topology of AD824 chip is seen in Fig. 3. A topology for aRD824 was designed to optime the size of a chip (see Fig. 4). Several chips aRD824 were produced at "Integral". Various standard tests on them were performed and compared to the datasheet of AD824.

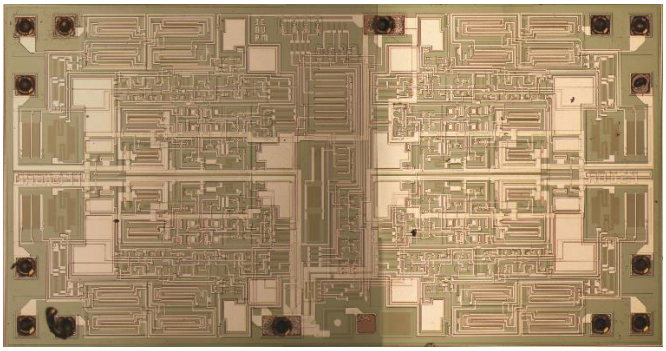

Fig. 3. **Topology of AD824 chip**

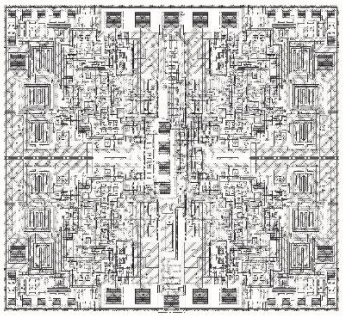

Fig. 4. **Topology of aRD824 chip**

Results and discussion

Simulation results of aRD824

The electric scheme of aRD824 was simulated in PSpice software. Results were compared to characteristics of AD824 as reported in their datasheet [2].

In Fig. 5 a measured open-loop gain graph of AD824 for various signal frequencies for supply voltage Vs = 5 V in no-load regime can be seen. In Fig. 6 a simulated open-loop gain graph of aRD824 is given, when there is no load, supply voltage + *Vcc* = + 5V, -*Vcc* = 0 V, and input voltage *Vinp* = 1 μV. It can be seen that frequency-gain graphs for AD824 and aRD824 are much similar.

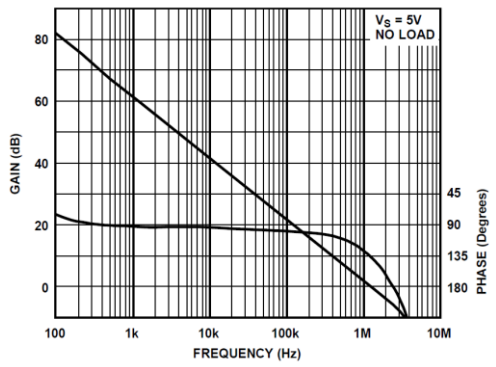

Fig. 5. **Open-loop gain/Phase, *Vs* = 5 V, no load; experimental data of AD824 (Fig. 5a. from [2])**

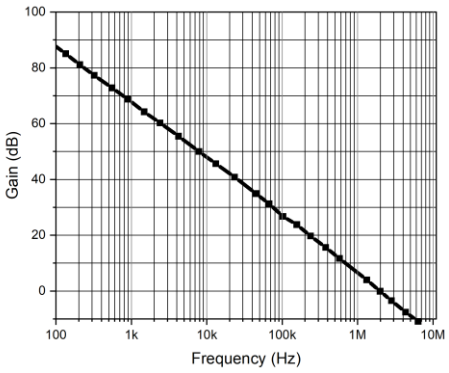

Fig. 6. **Open-loop gain, + *Vcc* = + 5 V, -*Vcc* = 0 V, no load; simulation of electric scheme of aRD824**

In Fig. 7 a small signal response graph of AD824 is given, when no load is applied and source voltage *Vs* = 5 V. In Fig. 8 a small signal response graph of aRD824 is shown, when no load is applied, source voltage + *Vcc* = + 5 V, and -*Vcc* = 0 V. The amplifier works best when the decline of the signal from a square waveform is not observed. It can be seen that both graphs are much similar.

In Fig. 9 a measured open-loop gain graph of AD824 for various signal frequencies for supply voltage *Vs* = 5 V and load capacitor *Cload* = 220 pF regime can be seen. In Fig. 10 a simulated open-loop gain graph of aRD824 is given, when there is a load capacitor *Cload* = 220 pF, supply voltage + *Vcc* = + 5 V, -*Vcc* = 0 V, and input voltage *Vinp* = 1 μV. It can be seen that open-loop gain vs. frequency graphs for AD824 and aRD824 are much similar.

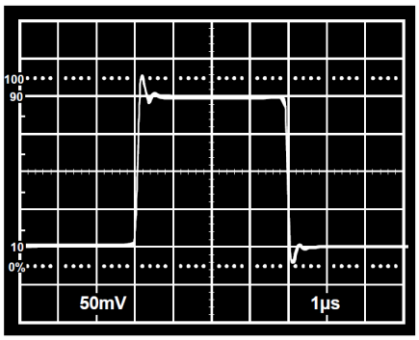

Fig. 7. **Small signal response, *Vs* = 5 V, no load; experimental data of AD824 (Fig. 5b. from [2])**

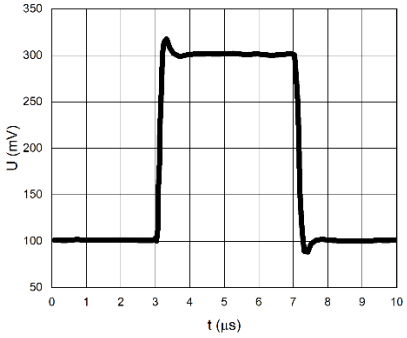

Fig. 8. **Small signal response, + *Vcc* = + 5 V, -*Vcc* = 0 V, no load; simulation of electric scheme of aRD824**

In Fig. 11 a small signal response graph of AD824 is given when the capacitor *Cload* = 220 pF is applied, and source voltage *Vs* = 5 V. In Fig. 12 a small signal response graph of aRD824 is given, when the load capacitor *Cload* = 220 pF is applied, source voltage + *Vcc* = + 5 V, and -*Vcc* = 0 V. The amplifier works best when the decline of the signal from a square wave form is not observed. It can be seen that both graphs are much similar, although the performance of aRD824 is better as signal oscillations are smaller. These graphs show less performance than similar graphs in no load regime (Fig. 7 and Fig. 8).

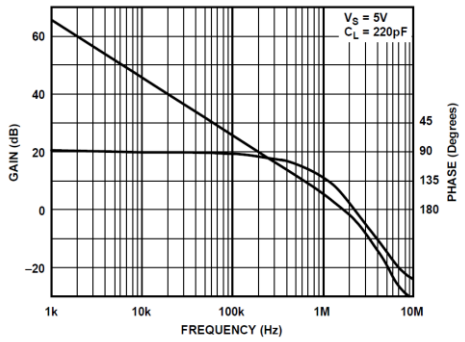

Fig. 9. **Open-loop gain/Phase, *Vs* = 5 V, *Cload* = 220 pF. Experimental data of AD824 (Fig. 6a from [2])**

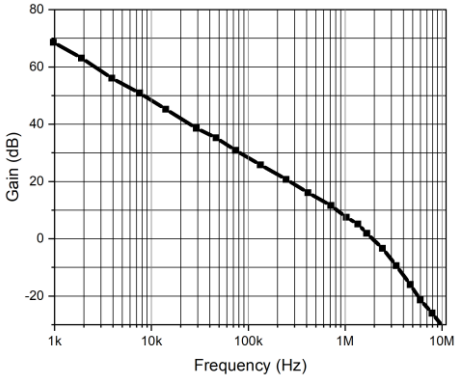

Fig. 10. **Open-loop gain, + *Vcc* = + 5 V, -*Vcc* = 0 V, *Cload* = 220 pF; simulation of electric scheme of aRD824**

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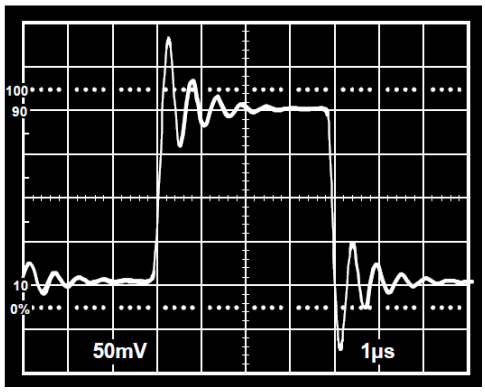

Fig. 11. **Small signal response, *Vs* = 5 V, *Cload* = 220 pF; experimental data of AD824 (Fig. 6b from [2])**

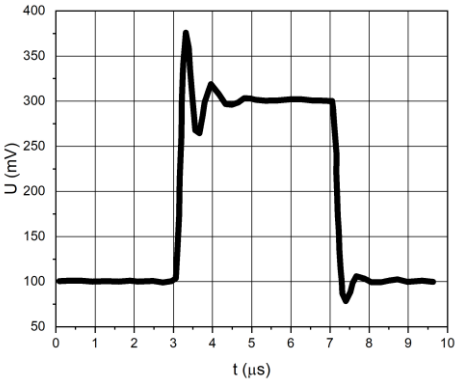

Fig. 12. **Small signal response, unity gain follower, + *Vcc* = + 5 V, -*Vcc* = 0 V, *Cload* = 220 pF; simulation of electric scheme of aRD824**

Operation amplifiers are characterized by a slew rate [12]. It is measured by applying a large signal step to the input of the operational amplifier and measuring the rate of change from 10% to 90% of the output signal's amplitude (see, for example, Fig. 13). For a rising signal, the slew rate can be calculated as:

$$SR_{01} = \frac{V_{out,90\%} - V_{out,10\%}}{t_{90\%} - t_{10\%}} \quad (1)$$

where SR_{01} – slew rate, measured in the rising signal arm, $V \cdot \mu s^{-1}$;
$V_{out,90\%}$ – output voltage value, when 90% of its saturation level is reached, V;
$V_{out,10\%}$ – output voltage value, when 10% of its saturation level is reached, V;
$t_{90\%}$ – time moment, when 90% of its output voltage saturation level is reached, μs;
$t_{10\%}$ – time moment, when 10% of its output voltage saturation level is reached, μs.

In Fig. 13 a measured slew rate output signal for AD824 is given for load resistor *Rload* = 10 kΩ. Its slew rate is 20 V/10.810 μs ≈ 1.85 $V \cdot \mu s^{-1}$. In Fig. 14 a simulated slew rate signal for aRD824 is given, when load resistor *Rload* = 10 kΩ is applied, source voltage + *Vcc* = + 5 V, -*Vcc* = 0 V, input voltage changes in the range *Vinp* = 0.2 - 4 V. In the rising arm, the slew rate is (3.65-0.55)/(5.01-3.24) ≈ ≈ 1.75 $V \cdot \mu s^{-1}$. In the declining arm, the slew rate is (3.65-0.55)/(13.19-11.27) ≈ 1.61 $V \cdot \mu s^{-1}$. Slew rates for AD824 and aRD824 are very similar.

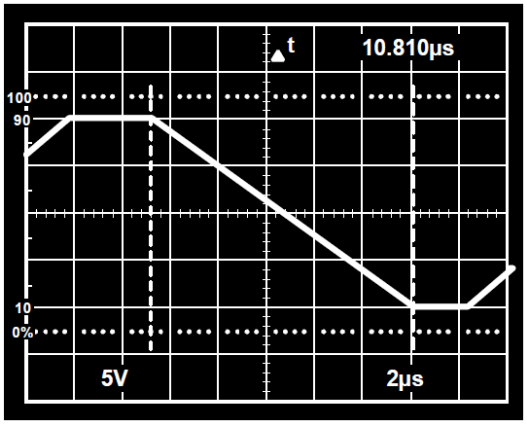

Fig. 13. **Slew rate, *Rload* = 10 kΩ; experimental data of AD824 (Fig. 8b from [2])**

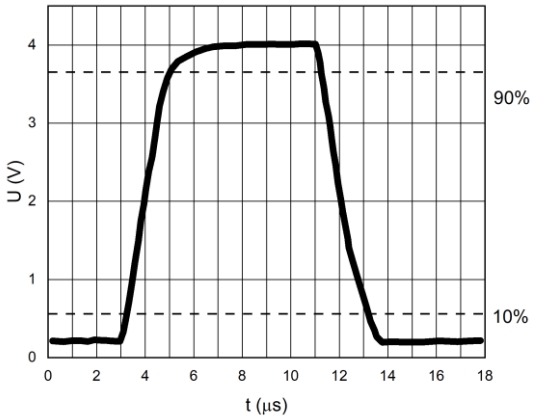

Fig. 14. **Slew rate, unity gain follower, + *Vcc* = 5 V, -*Vcc* = 0 V, *Vinp* = 0.2-4 V, *Rload* = 10 kΩ; simulation of electric scheme of aRD824**

In Fig. 15 a measured input bias current of AD824 for various temperatures for supply voltage *Vs* = 5V and 0 V regime is shown. In Fig. 16 a simulated bias current of aRD824 for various temperatures is given when source voltage + *Vcc* = + 5V, -*Vcc* = 0 V, and input voltage *Vinp* = 2.5 V. It can be seen that the input bias current vs. temperature graphs for AD824 and aRD824 are similar, yet with lower temperature sensitivity for aRD824.

In Fig. 17 a measured common-mode rejection of AD824 for various frequencies is shown. In Fig. 18 a simulated common-mode rejection of aRD824 for various frequencies is given, when source voltage + *Vcc* = + 5 V, -*Vcc* = 2.5 V, *Vcm_sin* = 1 V and no load is applied. It can be seen that the common-mode rejection vs. frequency graphs for AD824 and aRD824 are rather similar. Yet aRD824 shows larger values for frequencies below 1 kHz and smaller values for frequencies above 100 kHz. This difference may be minimized when comparing actual measurements from chips of AD824 and aRD824.

In Fig. 19 a measured power supply rejection ratio of AD824 for various frequencies is shown. The upper line corresponds to two polar supply voltage cases. The lower line corresponds to a single polar supply voltage case. In Fig. 20 a simulated and experimental power supply rejection ratio of aRD824 for various frequencies is given when source voltage + *Vcc* = + 4 V to + 6 V, -*Vcc* = 0 V, and no load is applied. It can be seen that the power supply rejection ratio vs. frequency graphs for AD824 and aRD824

are rather similar in shape. Yet, aRD824 shows larger simulation values for frequencies below 1 kHz. This difference is minimized when comparing the actual measurements from chips of AD824 and aRD824.

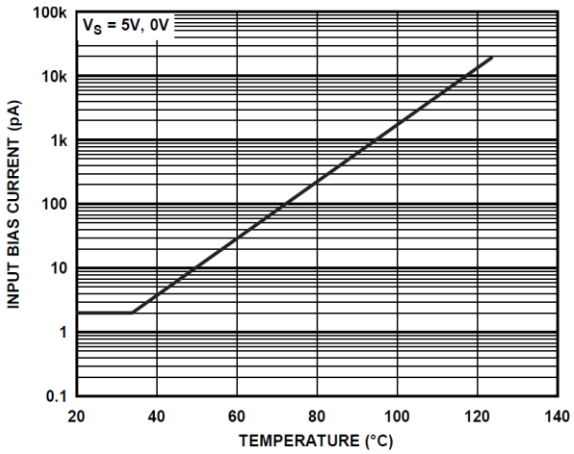

Fig. 15. **Input bias current vs. temperature, *Vs* = 5 V, 0 V; experimental data of AD824 (Fig. 17 from [2])**

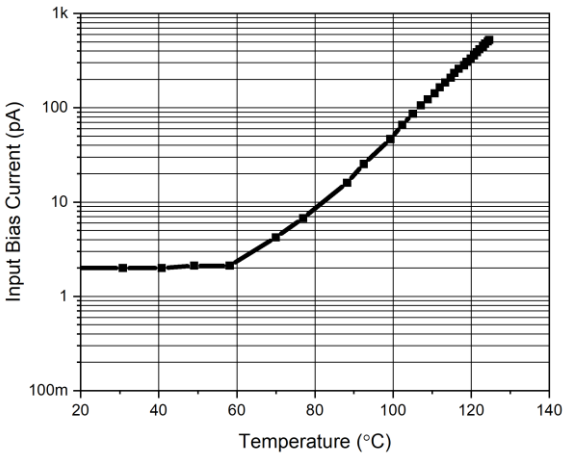

Fig. 16. **Input bias current vs. temperature, + *Vcc* = + 5 V, -*Vcc* = 0 V, *Vinp* = + 2.5 V; simulation of electric scheme of aRD824**

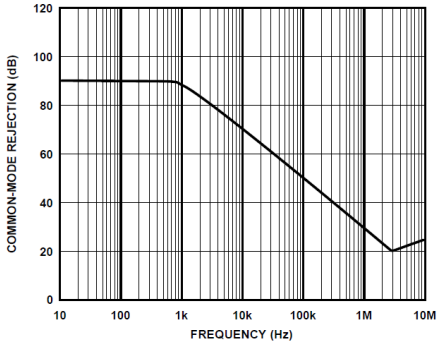

Fig. 17. **Common-mode rejection vs. frequency; experimental data of AD824 (Fig. 18 from [2])**

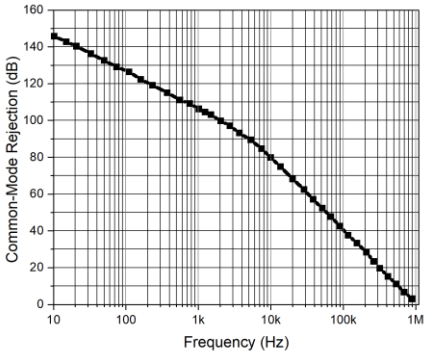

Fig. 18. **Common-mode rejection ratio vs. frequency, + *Vcc* = + 2.5 V, -*Vcc* = -2.5 V, *Vcm_sin* = 1 V, no load; simulation of electric scheme of aRD824**

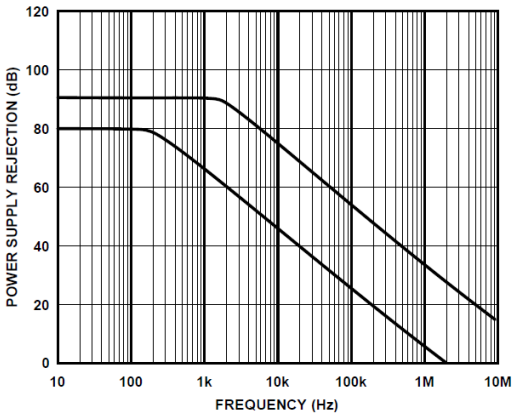

Fig. 19. **Power supply rejection vs. frequency; experimental data of AD824 (Fig. 22 from [2])**

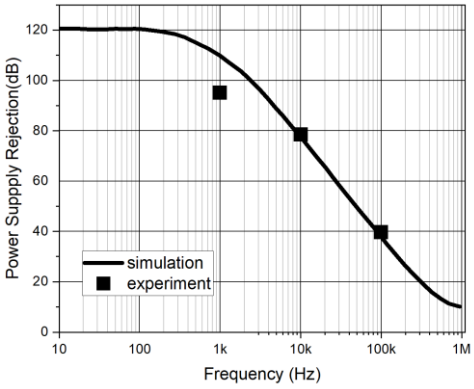

Fig. 20. **Power supply rejection ratio vs. frequency, + *Vcc* = + 4 V to + 6 V, -*Vcc* = 0V, no load; eimulation of electric scheme and experimental data of chip aRD824**

Measurement results of aRD824

Several characteristics of aRD824 chip were measured in experiments are given below. In Fig. 20 a measured small signal response of AD824 is given when load resistor 10 kΩ and capacitor 100 pF is applied. In Fig. 21 a measure of the small signal response of aRD824 is given, when source voltage + *Vcc* = + 5 V, -*Vcc* = 0 V, lead capacitor is 100 pF, and input voltage is changed as *Vinp* = 40mV to 80mV. It can be seen that small signal response graphs for AD824 and aRD824 are rather similar. Yet, aRD824 shows lower stability.

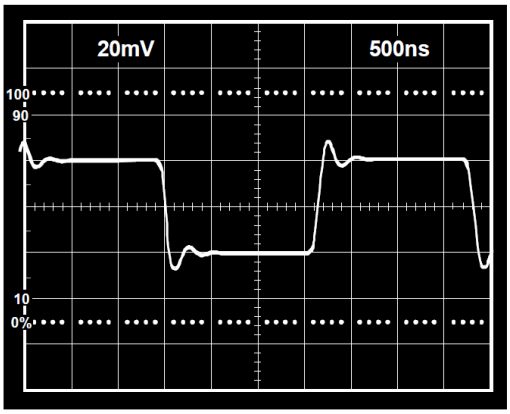

Fig. 21. **Small signal response, unity gain follower, 10 kΩ, 100 pF load; e xperimental data of AD824 (Fig. 26 from [2])**

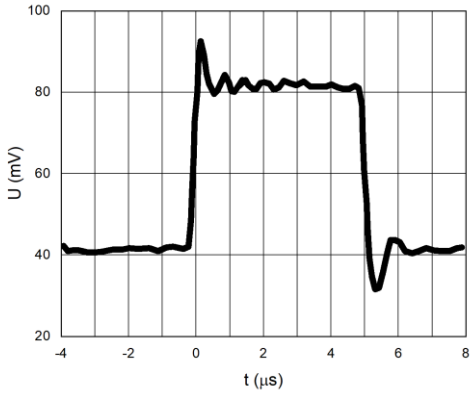

Fig. 22. **Small signal response, unity gain follower, + *Vcc* = + 5 V, -Vcc = 0 V, *Cload* = 100 pF, *Vinp* = 40 mV to 80 mV; experimental data of aRD824**

In Fig. 23 a measured open-loop gain and phase of AD824 for various frequencies is shown. In Fig. 24 a measured open-loop gain of aRD824 for various frequencies is given, when source voltage + *Vcc* = + 2.5 V, -*Vcc* = - 2.5 V, load resistor *Rload* = 100 kΩ and capacitor *Cload* = 15 pF is applied. It can be seen that the open-loop gain vs. frequency graphs for AD824 and aRD824 are rather similar. Yet aRD824 shows larger values for frequencies below 1 kHz and smaller values for frequencies above 100 kHz.

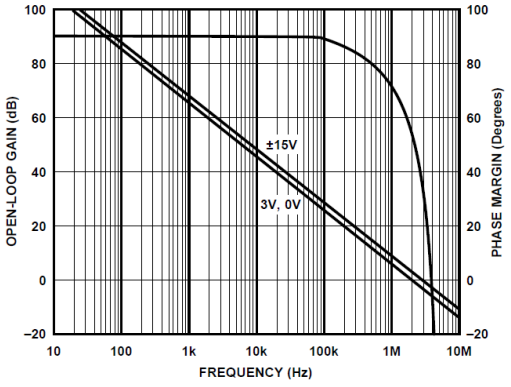

Fig. 23. **Open-loop gain and phase vs. frequency; experimental data of AD824 (Fig. 20 from [2])**

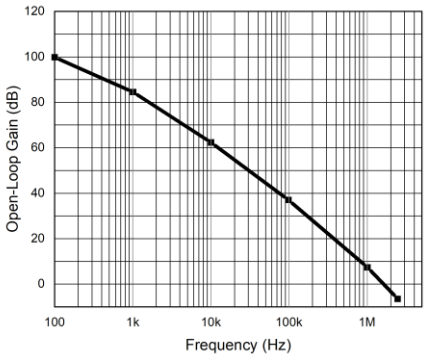

Fig. 24. **Open-loop gain vs. frequency, + *Vcc* = + 2.5 V, -*Vcc* = -2.5 V, *Rload* = 100 kΩ, *Cload* = 15 pF; experimental data of aRD824**

In Fig. 25 a measured output voltage to supply rail vs. sink and source load currents of AD824 is shown. In Fig. 26 a measured output voltage to supply rail vs. sink and source load currents of aRD824 is given, when source voltage + *Vcc* = + 5 V, -*Vcc* = - 2.5 V is applied. It can be seen that the output voltage to supply rail vs. sink and source load current graphs for AD824 and aRD824 are rather similar.

Additional parameters were measured on aRD824 chip. Open loop gain vs. *Rload* for + *Vcc* = + 2.5V; -*Vcc* = -2.5V was tested. The results are the following – gain of 120 dB for *Rload* = 100 kΩ, gain of 111 dB for *Rload* = 10 kΩ, and gain of 100 dB for *Rload* = 2 kΩ.

It was measured that for aRD824 chip, the voltage noise *Vn* p-p (0.1-10 Hz) ≈ 1μV. This is a good result as an expected target for aRD824 was its low voltage noise < 4 μV (Table 1, parameter No. 7).

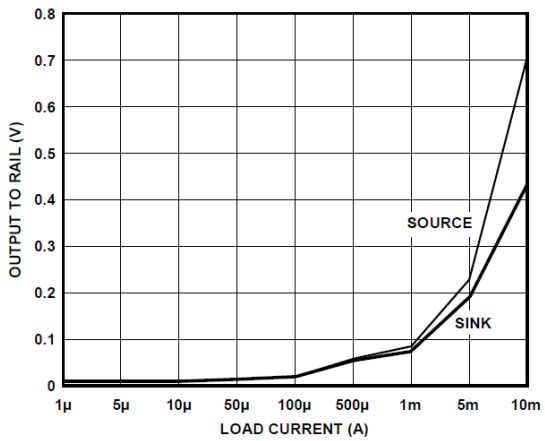

Fig. 25. **Output voltage to supply rail vs. sink and source load currents; experimental data of AD824 (Fig. 11 from [2])**

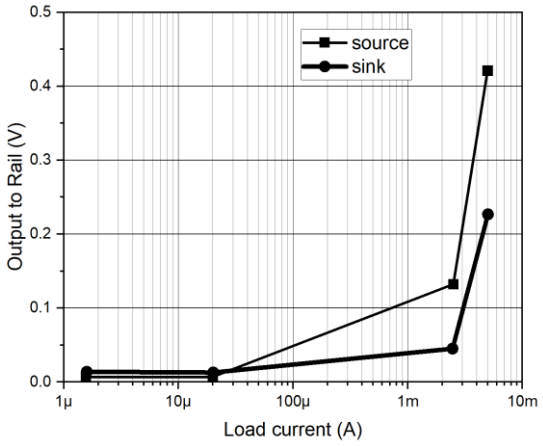

Fig. 26. **Output voltage to supply rail vs. sink and source load currents, + *Vcc* = + 5 V, -*Vcc* = 0 V; experimental data of aRD824**

Conclusions

The task of the research was to design, construct and test a 4-channel low noise rail-to-rail operation amplifier aRD824 with the specification given in Table 1, based on an initial prototype Analog Devices AD824 chip. Due to limitations and specificity of production processes in the production facility "Integral", the construction of the chip that is an implementation of an electric scheme of AD824 prototype is not applicable as a high rate of damaged chips may be obtained due to a failure to produce good performance FETs. Therefore, a modified electric scheme of AD824 prototype was proposed that allows to reach the expected specification. The electric scheme of aRD824 was simulated in PSpice software and data were compared to the datasheet of AD824. Simulated signals included – open-loop gain dependence on the signal frequency with no load, small signal response with no load, open-loop gain and small signal response for the capacitor load 200 pF, slew rate for 10 kΩ resistance load, input bias current vs. temperature, common-mode rejection vs. frequency, and power supply rejection vs. frequency. The results showed a high similarity of characteristics of the experimental AD824 and simulated aRD824 data.

A square topology of aRD824 was developed that is more compact than the rectangular topology of AD824. Chips of aRD824 were produced and tested on several performance indicators - power supply rejection ratio vs. frequency, small-signal response for load 100 pF and 10 kΩ, open-loop gain vs. frequency for load 15 pF and 100 kΩ, and output voltage to supply rail vs. sink and source load currents. The measured voltage noise for 0.1 Hz to 10 Hz signal input was 1 μV. The experimental results were compared to the datasheet of AD824 and showed high similarity.

A preliminary conclusion can be made that aRD824 achieves most of its planned performance parameters and can be accepted as a good analog to AD824. For the final conclusion, additional parameters of aRD824 should be measured to cover all characteristics given in the datasheet of AD824.

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Author contributions

Conceptualization, S.R. and M. L.; methodology, S.R., M.L. and D.K.; software, D.K.; validation, S.R.; formal analysis, D.K., S. R., M.L. and A.A.; investigation, D.K. and S.R.; data curation, D.K., S.R. and A.A.; writing - original draft preparation, A.A.; writing - review and editing, A.A., S. R. and D. K.; visualization, D.K. and A.A.; project administration, M.L.; funding acquisition, M.L. All authors have read and agreed to the published version of the manuscript.

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